MEMORY WITH AUTO REFRESH TO DESIGNATED BANKS

Abstract

A memory comprising 2^n dynamic random access memory (DRAM) banks, wherein n is an integer greater than or equal to 2, 2^n refresh row address counter circuits configured to generate 2^n sets of refresh row address signals in response to 2^n refresh enable signals, a multiplexer circuit configured to provide the 2^n sets of refresh row address signals to the 2^n DRAM banks in response to the 2^n refresh enable signals, and a bank select circuit configured to provide 2^n bank enable signals to the 2^n DRAM banks in response to at least $(n + 1)$ external address signals and in response to the 2^n refresh enable signals is provided. The 2^n bank enable signals cause at least two but less than all of the 2^n DRAM banks to be refreshed using at least two of the 2^n sets of refresh row address signals in response to the 2^n refresh enable signals.